CLAIMS

1. A computer system comprising

- a plurality of processing sets, each having at least one processor, and

- a bridge coupled to each of said processing sets and operable to monitor a step locked operation of said processing sets, wherein

- each of said processors has a processor identification register which is read/writeable and is operable to store in said register data representative of a processor identification, said processors being arranged, consequent upon a predetermined condition, to load a common predefined data value into said processor identification register.

2. A computer system as claimed in Claim 1, wherein said predetermined condition is a reset state of at least one of said plurality of processors.

3. A computer system as claimed in Claim 2, wherein said reset state is a state asserted in said fault tolerant computer system following boot or re-boot.

4. A computer system as claimed in any preceding Claim, wherein each of said processing sets includes a boot memory unit storing data which is representative of initialisation code arranged to initialise said processor to operate within said computer system, said boot memory unit including said common predefined data value which is loaded by said processor into said processor identification register.

5. A computer system as claimed in Claim 4, wherein said boot memory unit is a programmable read-only memory.

6. A computer system as claimed in any preceding Claim, wherein said common predefined value is an all zeros value.

7. A computer system as claimed in any preceding Claim, wherein each of said processors further includes

- a read only register having stored therein said process identification data.

8. A computer system as claimed in Claim 7, wherein said process identification data stored in said read only register is loaded, upon initialisation into said processor identification register.

9. A computer system as claimed in any preceding Claim, wherein said common predefined value is a processor identification of one of the processors of said fault tolerant computer system, said processor identification of each of said processors being matched.

10. A processor for use in a processing set forming part of a fault tolerant computer system, said processor comprising

- an interface for communication with an I/O bus, and

- a process identification register which is read/writeable, and has stored in said register data representative of a processor identification, wherein said processor is operable, to write a common predefined data value received via said I/O bus into said processor identification register.

11. A processor as claimed in Claim 10, comprising

- a read only register having stored therein said process identification data, wherein said process identification data stored in said read only register is loadable, upon initialisation into said processor identification register.

12. A method of operating a fault tolerant computer system comprising a plurality of processing sets, each of which processing sets is connected to a bridge, each of said processing sets having at least one processor, said method comprising the steps of;

a) detecting a predetermined condition representative of a state in which said processor identification is present in a process identification register of said processor; and

b) loading a common predefined data value into said processor identification register of each of said processors which predefined data value has an effect of masking said processor identification.

13. A method of operating a fault tolerant computer system as claimed in Claim 12, wherein said predetermined condition is a reset state of at least one of said plurality of processing sets.

14. A method of operating a fault tolerant computer system as claimed in Claim 13, wherein said reset state is a state asserted in said fault tolerant computer system following boot or re-boot.

15. A method of operating a fault tolerant computer system as claimed in Claim 12, comprising

detecting an error condition of at least one of said plurality of processing sets, and

if said error condition is detected performing the step of loading said common predefined value in said processor identification register of said at least one processor of the processing set which has said detected error.

16. A method of operating a fault tolerant computer system comprising a plurality of processing sets, each having at least one processor, and a bridge coupled to each of said processing sets and operable to monitor a step locked operation of said processing sets, said method comprising the step of

- replacing a processor of one of said processing sets with a replacement processor according to Claim 10.

17. A method of operating a fault tolerant computer system as claimed in Claim 16, wherein said replacement processor is replaced by

- replacing one of said processing sets with a processing set having the replacement processor according to Claim 10.

18. A computer system as herein before described with reference to the accompanying drawings.

19. A processor as herein before described with reference to the accompanying drawings.

20. A method of operating a fault tolerant computer system as herein before with reference to the accompanying drawings.